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8T SRAM Cell with Open Defects under Voltage and Timing Variations

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***Abstract*— The defective behavior of an 8T SRAM cell with resistive open defects located in different nodes on the read port is presented. A simple array made up of 4x4 cells is considered in order to characterize the effect of the defective cell in the array. The impact of the defect has been analyzed at the electrical level and the implications at the logic level have been classified. Due to the similarity between the classical 6T SRAM cell and the studied 8T cell, only defects affecting the read port transistors have been considered. In the paper, it is shown how a resistive open defect may influence the correct operation of a reading action on the selected cell. Furthermore, the sequence of read and write operations needed to determine each location of the considered defects are analyzed. Timing conditions and power supply voltages are considered for the characterization. Different orders of magnitude for the critical resistance are found depending on the case. A 65nm CMOS technology has been used for the illustrative example presented in the work.**

Keywords- Resistive Open Defect; 8T SRAM cell; read error; defect analysis; critical resistance.

I. INTRODUCTION

Requirements of memory to store data and instructions are increasing every day. In nowadays designs, the area occupied by SRAMs is higher than the rest of the IC (Integrated Circuit) and this fact is growing for each new technology node.

The aggressive scaling of SRAM cells decreases the reliability of operation of the memory cores due to an increasing impact of the variability of the process parameters. The International Technology Roadmap for Semiconductors (ITRS) 2009 [1] reports an increase of three orders of magnitude in the variability-induced failure rate when scaling High Performance SRAM from 45nm to 32nm. The study assumes the traditional 6T cell design with the same auxiliary circuits (pMOS and nMOS ratios, sizing and required read/write circuits, etc).

Weak resistive open defects pose threat on reliability [2] Based on Poisson distribution, resistive open defects of small size are more probable than larger size defects [3][4] and, thus, non-catastrophic defects, which degrade the response of circuit but do not produce a catastrophic behaviour, are more probable than full open defects.

Most of the current defect based memory test algorithms are centered on the 6T (six transistors) cell circuit which is the dominant present architecture for commercial embedded SRAM cores. The 6T SRAM shares the bit lines for the read and write operations. To guarantee an acceptable SNM during READ operations, the strength of the access nMOS transistor must be low compared to the strength of the pull-down nMOS. On the other hand, to assume an acceptable SNM during write operations, the strength of the access nMOS transistors must be high compared to the strength of the pull-down nMOS. These conflicting requirements are acceptable for cells with large SNM, but in the near future, with lower margins, the cell becomes unreliable.

To overcome this problem in future technology nodes, for 32nm and beyond, the 8T SRAM cell has been proposed as a possible substitute of the 6T SRAM cell . In the 8T cell, the electrical paths activating read and write operations are independent thanks to adding a Read Word Line (RWL), a Read Bit Line (RBL) and two transistors connected in series as illustrated in Figure 1. .

In this paper, we focus our attention to resistive defects located on the read port of the 8T SRAM cell. Defects at the six remaining transistor are assumed to behave similarly to the classic 6T cell, which have been widely researched in recent years [5].

The rest of the paper is organized as follows: Section II reviews the 8T cell circuit architecture. The effect of resistive defects is presented in Section III. A classification of the characterized defective behaviors is listed in Section IV, and finally, the conclusions of the work are presented.

II. 8T SRAM CELL

The structure of an 8T SRAM cell [7]-[9] is derived from the classical 6T SRAM cell. The basic difference between them is the separation between the read and the write active signals, named Read Word Line (RWL) and Write Word Line (WWL), respectively (see Figure 1.). In order to achieve this separation, two stacked NMOS transistors for a single-ended read action are added (labeled RDaux and RD in Figure 1.). In normal operation, RDaux transistor is activated through signal RWL in order to perform a read action on the memorized bit (Q). Assuming that the Read Bit Line (RBL) has previously been pre-charged to a high value (V_{DD}) before the reading operation, the RBL node will keep the high

voltage if a memorized state Q=1 (i.e. nQ=0) had been written in the cell. In the case of Q=0, the high voltage (nQ=1) feeding the RD transistor's gate allows the discharge of the RBL thought the two stacked *on* transistors.

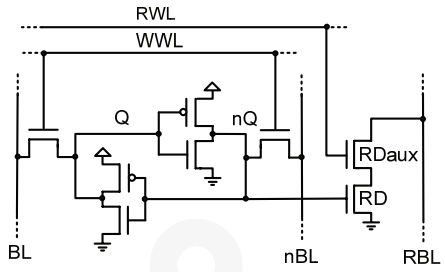


Figure 1. Schemmatics of the considered 8T SRAM cell.

In a typical SRAM structure made up of 8T cells [7], the memorized data is sensed in a single ended way and a number of 8/16/32/64 bitcells are connected to a local bit line (LBL) as a dynamic logic gate. Figure 2. illustrates a part (4x2 cells) of the considered structure of 4x4 cells. When the RWL is turned *on*, depending on the data stored in the cross coupled inverter pair, read bit line (RBL_{ij}) of the cell is evaluated, and thought it, the LBL node is updated. Next, the voltage of the local bit line sensing is applied to another stage of the dynamic gate structure consisting of Global Bit Line (GBL). Bitline sensing is performed hierarchically using dynamic logic gates. A weak PMOS transistor called 'keeper' tries to pull up the dynamic node voltage (V_{LBL}) to V_{DD}.

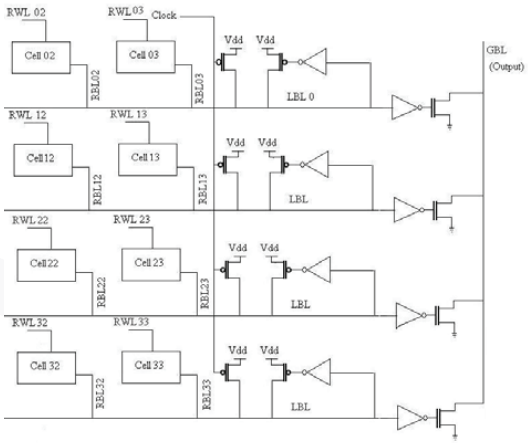


Figure 2. Part (4x2) of the total 4x4 SRAM cell matrix under study: hierarchy reading structure.

The SRAM array considered in this work is based on a square 4x4 structure (see Figure 3. for the writing connections schematics). By using this simple array, the effect of a defective cell will be propagated to any of the cells sharing the local or the global reading circuitry.

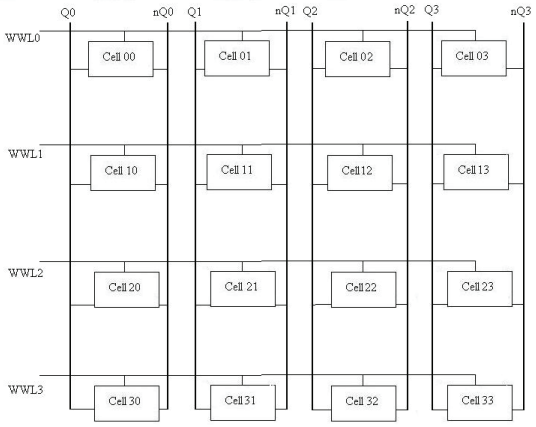


Figure 3. Schemmatics of the write circuitry of the 4x4 structure 8T SRAM cell considered.

An example of the synchronization between the signals involved in the writing and reading operations performed on the cells is illustrated in Figure 4. . In the figure, the (low) clock signal (CLK) is responsible for precharging the local bit lines (LBL_i) of the block. The reading action, activated through a high voltage on (RWL_{ij}), is applied after the precharge has been concluded. Note that since read and write access to the selected cell are independent of each other, precharging local bit line and activating a read action on a cell can be done simultaneously, as illustrated in Figure 4. . WWL and RWL signals are activated during a percentage of the clock signal.

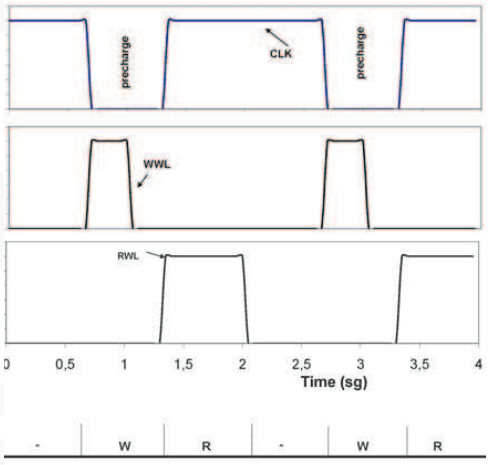


Figure 4. Impulse wave inputs: (a) Clock Signal; (b) Write Word Line; (c) Read Worl Line

A CMOS 65 nm STMicroelectronics technology has been used to implement the memory, and nominal V_{DD}=1.2V and clock period T=1ns have been assumed.

In the next section, the assumption of open defects affecting the read port of any of the 4x4 array of 8T cells is done.

III. DEFECTIVE 8T SRAM CELL

In this section, resistive open defects affecting the terminal nodes of the read port transistors are considered. Throughout the characterization, the written values on the cell are assumed to be electrically within specifications since the defects only affect the read port. Three different locations have been considered for the defects, as illustrated in Figure 5. . Open O1 affects the node driving the gate of transistor RDaux, O2 assumes a partially broken line at the gate of transistor RD, while O3 is located on the discharge direct path from LBL and ground.

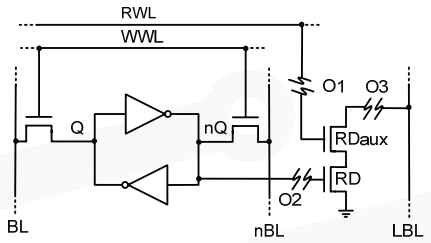


Figure 5. Defect open locations considered on the read port of the cell.

In order to characterize the effect of the open defects [10], the partially broken connections affecting each node will be modeled by a resistance Rop.

A. *Resistive open defect at the gate of RDaux transistor*

In this section, the resistive defect located at the gate of RDaux transistor (see Figure 5.) is analyzed. The mission of this transistor is to sense the cell data (though RD transistor) to the Local Bus Line (LBL).

Every cell is controlled by its local RWL signal as shown in Figure 2. . Thus, RWL_{ij}, is activated if the cell placed in row *i* and column *j* is the one selected. In this case, RWL_{ij} is connected to the general RWL signal. Depending on the previously written value, there are two possible scenarios (see Figure 6.). In the first case, if the memorized data is a high value (Q=1, i.e. nQ=0), the RD transistor is *off*, and the RBL line will not be discharged. In this case, the state of the RDaux transistor does not affect the correct behaviour of the cell. In the second case, if the written data is a low value (Q=0, i.e. nQ=1), the RD transistor is *on*, and the RBL line would be discharged in a defect-free cell. In the case of a defective cell with open O1, the gate of the RDaux transistor is not properly connected to the expected RWL logic high signal value.

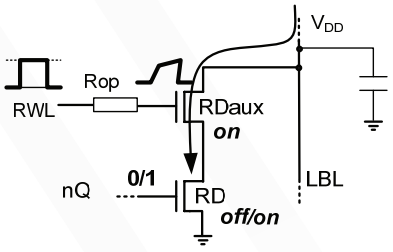
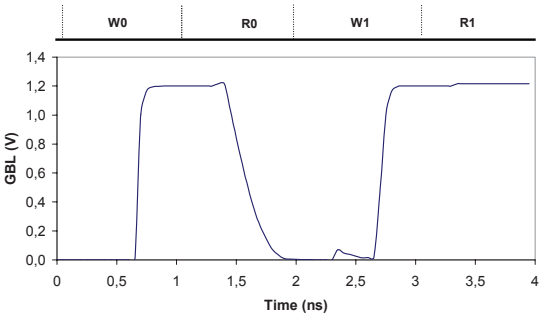
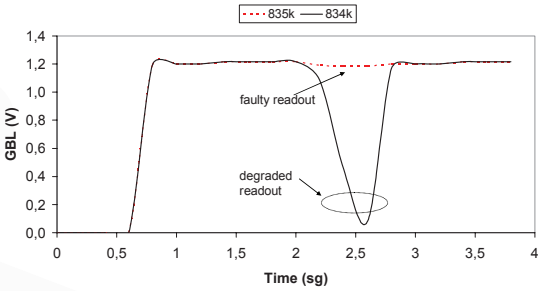


Figure 6. Electrical model of the defective 8T SRAM cell with O1.

In order to characterize the behavior of the cell, let us assume that the defective cell is addressed and a series of four basic operations are applied to the block, namely, writing Q=0 (W0) followed by a readout of this low state (R0), and writing a high state Q=1 (W1) followed by its readout (R1). The defect-free behavior of GBL for the write and read actions (R0, W0, W1, R1) is illustrated in Figure 7. a. However, the resistive open defect is expected to hamper the connection of RDaux and, thus, makes it difficult to discharge the local bit line (and the global bit line) provided Q=0. Depending on the Rop value, the read port of the addressed defective cell succeeds in discharging the LBL and, as a consequence, the output of the whole block, GBL, too. Figure 7. b shows the voltage at GBL for two different Rop values, one of which (835kΩ) causes an erroneous readout R0 since the GBL is not discharged after the period time of the working frequency. In the same figure, Rop=834kΩ allows a correct (although degraded) readout of the previous writing action (W0) performed on the cell.



a)



b)

Figure 7. GBL behaviour for a series of R0, W0, R1 and W1 actions on the cell with open O1: a) Defect-free behaviour and b) degraded or even errouneous response depending on the Rop value.

The Rop that causes the readout of the cell to flip between the correct GBL (although degraded) response and the erroneous outcome is on the order of 835kΩ in the case of the nominal working values assumed in the example (ie, period of the clock signal T=1ns, and voltage supply V_{DD}=1.2V). This resistance is named *critical resistance,* Rcr, and its dependence on the clock period is illustrated in Figure 8. . The longest the

working period is, the higher the critical resistance Rcr is. The reason for that dependence is the fact that the discharge of the parasitic capacitance created on GBL line is performed over a longer period of time (provided the period is longer) and the increase in the RC delay is compensated. However, the Rcr dependence on the power supply voltage is not lineal since there is a tradeoff between the current strength of (defective) transistor RDaux and the charge to be eliminated from C_{LBL} (see Figure 8.).

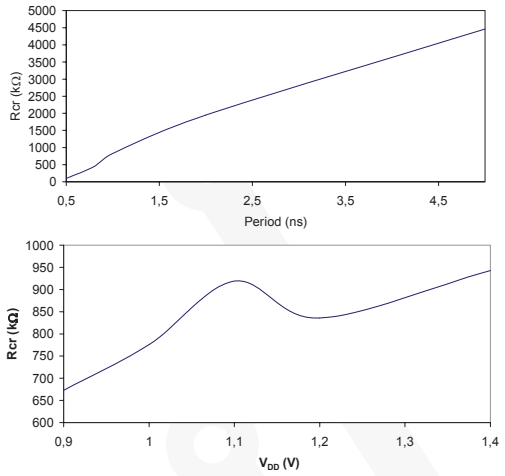


Figure 8. Open O1: a) Relantionship between the critical resistance Rcr and the period of CLK, b) critical resistance dependence on power supply V_{DD}.

According to the results shown in the previous figure, the widest range of resistive open defects at the gate of RDaux transistor is detected at the fastest working frequency. Similarly, the lowest the voltage supply value is, the widest range of detected open defects is obtained. Rcr is more sensitive to the working period.

B. Resistive open defect at the gate of transistor RD

In this section, the effect of an open defect located at the gate of the RD transistor is presented. This transistor allows the discharge of the pre-charged LBL output depending on the memorized state. In the case of Q=1 (i.e. nQ=0), RD is kept *off* and the discharge of $C_{LBL}$is not allowed, forcing the output to stay in the high level acquired after the pre-charge done before the read action. But if Q = 0 (i.e. nQ = 1), RD turns *on* and the output is discharged thought the two series transistors RDaux and RD. In the case of a resistive O2, RD becomes weakly *on* or even is kept *off* depending on the resistive value of the defect and, thus, the output signal may be sensed as logic high. The defective behaviour of the cell is similar to the case of O1, ie, resulting in a R1 when a R0 is expected. However, for defect O2, the critical resistance range is found around higher values than in the case of O1. Indeed, Figure 10. illustrates the case of two Rop values close to the critical value, which lies around 6,7 GΩ, for the same sequence of write and read actions shown in Figure 7. , ie (W0, R0, W1, R1). Figure 10. and c show the dependence of the critical resistance versus the period time and the power supply, respectively. As for the O1 case, the lower the values for the two parameters are, the wider the detected defects range is obtained.

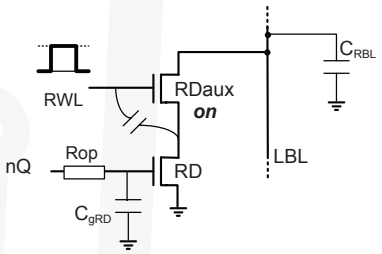


Figure 9. Resistive Defect at Gate of RD Transistor

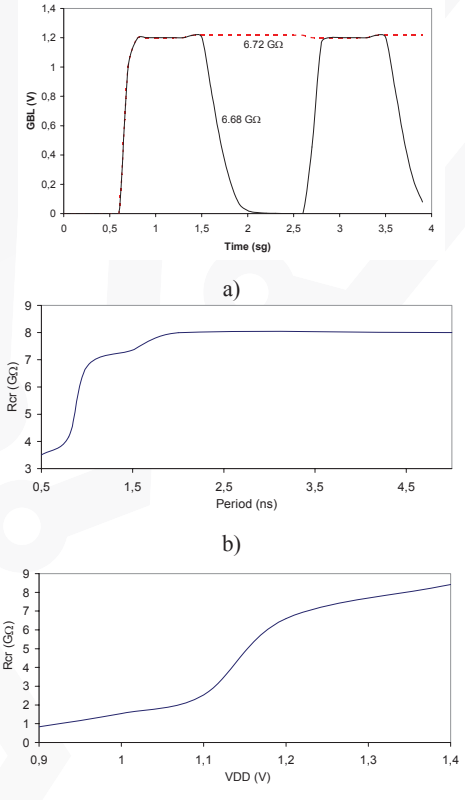


Figure 10. a) Bevahior of the 8T SRAM cell with defect O2 for two Rop around the critical value, and Rcr dependence on b) the period time of the clock and on c) the power supply voltage.

Although open defects O1 and O2 are quite similar in topology, the signals that control them are different (O1 is driven by RWL, which is connected to logic 1 during a percentage of the clock period). However, the voltage driving O2 depends on the previous value (nQ) memorized in the cell and the number of periods lasted since this last writing action

on the defective cell. Depending on this history effect on the parasitic capacitance C_{gRD}, the readout of the cell may change for a given open defect. Figure 12. shows the slow discharge of C_{gRD} due to the resistive defect O2 for a nQ change from 1 to 0. For this particular example, the charge accumulated in C_{gRD} allows RD to be kept *on* and thus discharge the LBL (causing a faulty R0 readout as illustrated in Figure 12. The dependence of Rcr versus the period and the power supply voltage are illustrated in Figure 12. b and c for this particular case where there is a change in the memorized state of the cell (as in Figure 11.

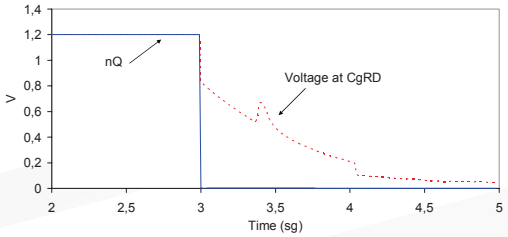


Figure 11. Voltage at the gate of the RD transitor for a change in the memorized state of the cell from Q=0 to Q=1. Rop=642k. Glitches are due to the coupling between the gate node to RWL.

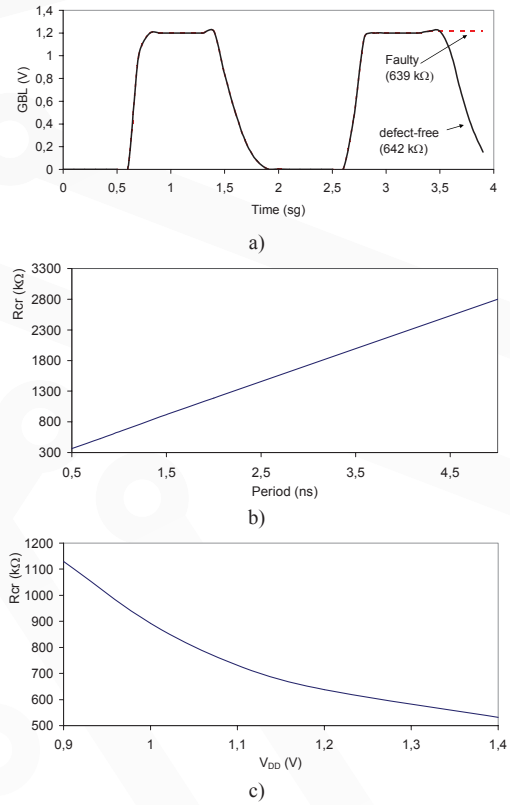


Figure 12. a) Bevahior of the 8T SRAM cell with defect O2 for two Rop around the critical value and a change in the Q state as in Figure 11. , and Rcr dependence on b) the clock period and c) on the power supply voltage.

C. *Resistive open defect at the direct path of the read port*

In order to characterize the defective behavior of the cell with O3 (Figure 13.) let us analyze what happens when a defect is located between the drain of RDaux transistor and the local bit line LBL. According to the analysis presented for O1 and O2, the output line LBL is pre-charged prior to the reading action triggered by RWL. In the case of Q=0, the LBL node will be discharged through the two series transistors RDaux and RD in a defect-free circuit. However, the existence of O3 hampers the discharge of LBL and the output GBL will keep the pre-charged value. The larger the resistance of the open is, the longer the LBL is needed to discharge the previously accumulated charge (see Figure 14. .

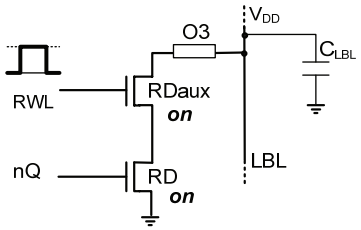


Figure 13. Open defect O3 located on the direct path between LBL and ground.

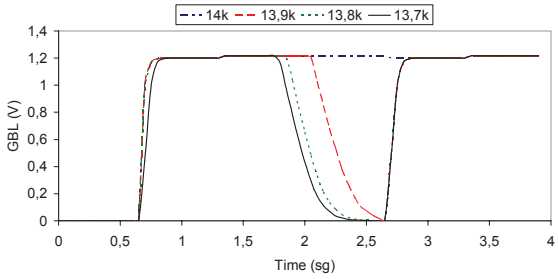


Figure 14. a) Bevahior of a cell with defect at O3: (a) response; (b) in depends of time; (c) in depends of power supply

The critical Rcr for open O3 located in the direct path of the read port lies around 13,8 kΩ for a wide range of period times (see Figure 15. a). This weak dependence on the period time is due to the fact that the time activating signal RWL is proportional to the total period and an increase in Rop is compensated by this longer activating time. However, the Rcr dependence on the power supply voltage is a decreasing function since there is a tradeoff between the charge that must be eliminated from the LBL and the current capability of the Rop in series with transistors RDaux and RD, resulting in this decreasing behaviour.

IV. DEFECTIVE BEHAVIOR CLASSIFICATION

According to the simulation results presented in this paper, some detectability conditions can be derived for resistive opens affecting the read port of an 8T SRAM cell located inside an array of similar and defect-free cells. Note that the target cell works properly as far as the writing operation is

concerned. Only the read operation has been analyzed. Table I summarizes the critical resistance and the LBL/GBL behavior for all the cases (opens O1, O2 and O3), assuming nominal power supply V_{DD}=1.2V and working frequency 1MHz (T=1ns).

In relationship with the most suitable timing and power supply values for the detection of the defect on the cell, in general, the fastest clock period allows the detection of a wider range of resistive open defects. As far as the power supply value is concerned, both lower and higher than the nominal voltage should be combined in order to defect the widest range of open defects in the read port of the defective cell.

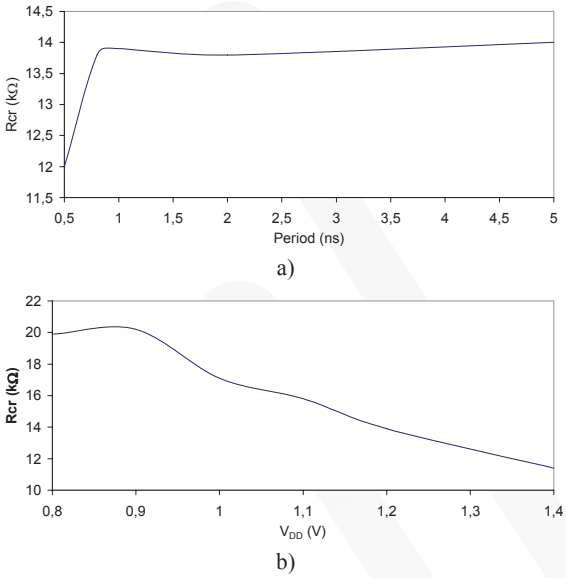


Figure 15. O3: Dependence of Rcr versus a) the period time of the clock, and b) the power supply value.

TABLE I. CLASSIFICATION OF THE GBL READOUT OF THE 8T SRAM ARRAY FOR OPEN DEFECTS IN THE READ PORT OF ONE CELL

Open defect	*Rop*	Read or write Action	
		R0	***R1***
O1	< 833 kΩ	Ok	Ok
	> 833 kΩ	defective	Ok (degraded)
O2	< 639 kΩ	Ok	Ok
	> 639 kΩ < 6.75 GΩ	Ok	defective (after R0)
	> 6.75 GΩ	defective (after R1)	defective (after R0)
O3	< 13.9 kΩ	Ok	Ok
	> 13.9 kΩ	defective	Ok

V. CONCLUSIONS

The effect of a defective cell in an array of 4x4 8T SRAM cells has been classified for different timing and power supply conditions. Due to the similarity between the classical 6T SRAM cell and the 8T cell, only defects affecting the read port transistors have been considerer. It has been shown how these resistive defects can affect the cell readout, and how for resistance defects higher than a critical value, these defect can escape detection. Different orders of critical resistance have been found, namely, hundreds of kΩ for open O1, hundreds of kΩ or units of MΩ for O2 depending on the transition performed on the memorized bit, and tens of kΩ for O3. As far as the most suitable timing for the defection of the defects is concerned, fast working frequency has been found as the able to defect the widest range of resistive opens. Furthermore, a combination of low and high power supply voltage has been proposed for the best detection scenario. The presented readout classification will be used in a future work in order to evaluate the optimum test sequence applied to 8T SRAM memories.

ACKNOWLEDGMENT

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